

Single-Chip Instrumentation Module for Radiation Environment

Robert L. Shuler
NASA Johnson Space Center
Avionic Systems Division / EV131
Houston, TX 77058
rshuler@ems.jsc.nasa.gov, 281-483-5258

Abstract - This paper describes design philosophy and test results for a dual channel single-chip instrumentation interface, having a daisy-chain serial output, on-chip programmable signal conditioning, on-chip programmable low pass filtering as low as 10hz, and A/D conversion. The device is designed to be latchup-free in a low earth orbital environment, to avoid state information that would allow SEU errors to corrupt more than one sample, and to be fabricated using the commercial CMOS14TB (HP 0.5 μ) process available through MOSIS.

1 Introduction

Acquisition of sensor data is a common task on-board spacecraft. Often the sensors are widely distributed, and require a variety of gain, filter and other settings for proper acquisition. Traditional approaches use multiplexor-demultiplexor modules (MDM's) processing tens to hundreds of measurements, each being linked by some sort of avionics bus to a main processor. Customizable cards plug into the MDM to handle the unique signal conditioning requirements of each sensor.

The bulk and mass of the MDM's and the shielded cable connecting each sensor to its MDM can pose a serious constraint to the design of both large and small spacecraft, but more so for small spacecraft, for sensor intensive applications such as touch-sensitive robots, and for wireless instrumentation. This paper presents the design of a monolithic device intended to resolve many of the above described problems. The design of two test chips will be presented, along with test results from the first, and directions being pursued for a third.

2 Functions

Foremost of the required features was incorporation of all functions in silicon. External capacitors or resistors were not desired. Functions necessary to interface sensors include:

- programmable input sensitivity (gain) ranging from a few millivolts for low level strain gauges, to a few volts for other devices.
- differential input for sensors with 2 floating terminals (bridge based)

- low offset (order of 100 microvolts)
- anti-alias filtering, with cutoff ranging from 500 Hz down to a few Hz
- 10 bit or better A/D at 1000 samples/second, synchronizable
- serial digital output

The device must function acceptably for semi-critical systems in a low earth orbit radiation environment. This will be taken to mean latchup should be avoided, and a single event upset (SEU) should affect no more than one set of samples. In addition, it is desirable to be able to integrate the functional subsystems of the device into larger ASIC's with minimal re-engineering, that is, they should be usable with automatic routing tools without undue performance or noise margin degradation.

3 Design for Radiation Tolerance

The strategy for latchup prevention was based on recent test results from the Aerospace Corp. [1] which suggest that a single p++ guard band around n-type devices creates an adequate barrier in HP 0.5 μ . Each layout cell was drawn with a complete guard band, except for analog cells containing no n-type devices. The digital cells were derived from a different cell library having no lateral guards and designed to be capped at row ends. Each cell was individually capped, and the position of the cap became a de facto standard of the cell design for the mixed library. An example abutment of an analog and digital cell is shown in Figure 1. Note that minimum-width poly crossings of the guard bands were allowed, but that care was taken not to leave any floating islands.

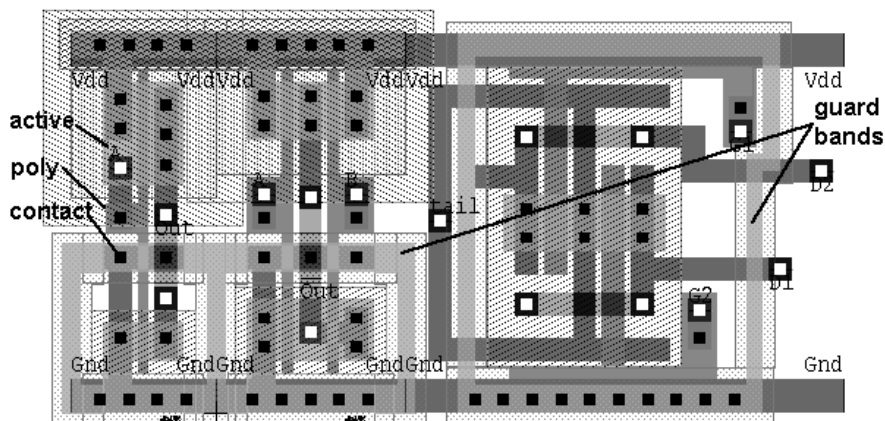


Figure 1 - Guard Band Example

The strategy for dealing with SEU in the first two test chips, ANAC1 and ANAC2, was to include no state information that was required to be retained from one sample to the next.

Programmable gain and filter inputs are discrete inputs, and the command to begin a sample performs a general reset of the serial digital output and A/D circuitry. In this way, an SEU can corrupt only a single time point, and software can check adjacent points for corroboration of any unusual values.

In planned follow up chips, the discrete program inputs will be replaced by stored configuration data coming in over the digital serial bus. For this, SEU resistant flip flops must be used, either the synchronous flip flops developed at the University of New Mexico [2], or others under development at JSC.

4 Building Block Architecture

In order to permit automatic place and route, while maintaining matching conditions, all components requiring matching were paired together in uniform height standard cells. For example, one cell might contain an n-type differential pair of FET's, and another might contain a pair of resistors. Silicide block was used for all resistors. A schematic symbol was created for each block, and used to build a netlist that was used both for simulation and to direct the place and route.

For the first two test chips, related functions, such as one of the front-end instrumentation amps, or one of the filter stages, were routed together into a macro-block. Such a block might have 5 to 7 rows of standard cells, and would be formatted as a very large standard cell. All macro blocks were the same height. This forced localization of routing for each functional unit. For the most part, digital logic was segregated into separate macro-blocks. Once the macro blocks were formed, the final chip was produced by automatically placing and routing them.

The cap-well was used to make linear capacitors. Large value 80 pF capacitors were drawn as a macro-block, which was somewhat inconvenient from a netlist standpoint, but made an effective layout.

For the second test chip, ANAC2, some RC decoupling was built into the frame of each macro block, in an attempt to improve the Vdd isolation between macro blocks. An example macro-block is shown in Figure 2.

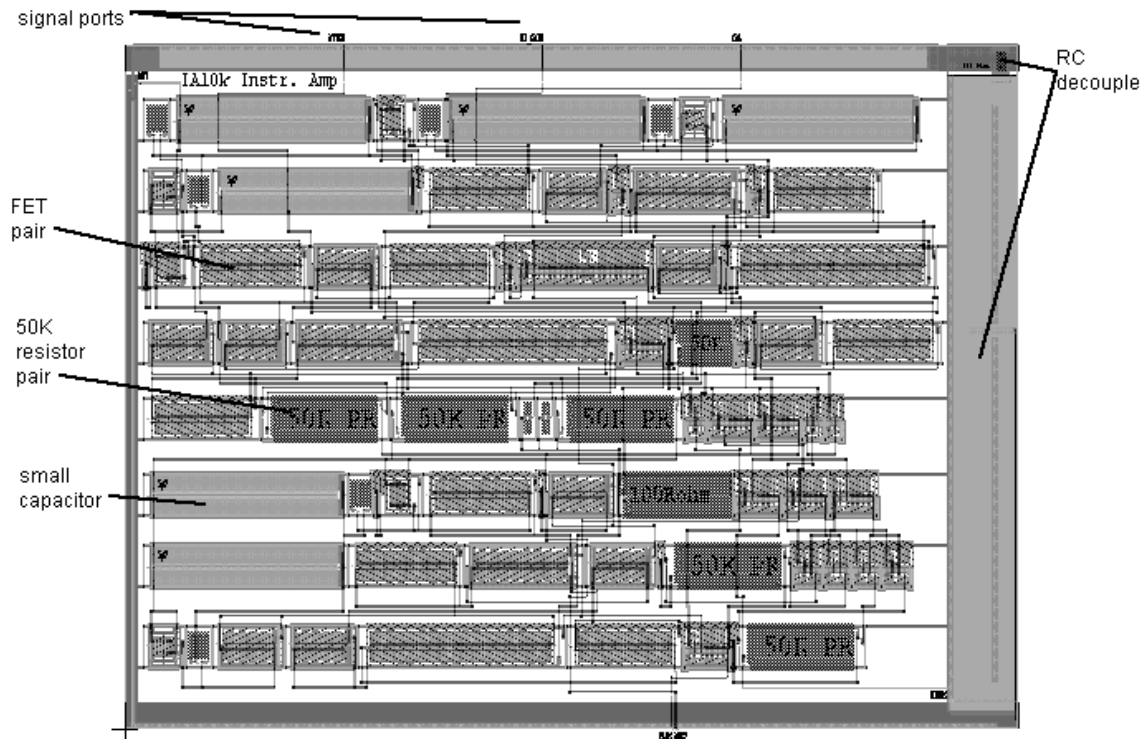


Figure 2 - Macro-Block Example (IA10K Instrumentation Amp)

5 Op Amps

In the first test chip, ANAC1, a simple differential op amp circuit with rail-to-rail drive capability was used. This circuit is similar to one obtained from Tanner Research [3] originally designed for implementation in 2.0μ CMOS, but with fewer output stages due to the difficulty of compensating it properly in the HP 0.5μ process. This resulted in an amp whose simulated gain into the required loads marginally qualified as an op-amp. Test results from ANAC1 showed the gain to be somewhat less than predicted, and not suitable.

ANAC1 had a provision for external bias, and it could not be adjusted to simultaneously achieve reasonable gain and reasonable offset. However, at favorable settings, not only was the offset a reasonable 2 millivolts average (for the instrumentation amp configuration, which performs cancellation of systematic offset), but was constant within 0.2 millivolts over long periods of time (quarter of an hour). This suggested that some further adjustment of transistor sizes for better matching coupled with an output stage would produce an op-amp module that met our requirements.

In the second test chip, ANAC2, two channels were present, and a different op amp configuration was tested in each channel. In the first channel, a module called OP10K was used, derived from the earlier op amp, as shown in Figure 3. In the second channel, a

very basic op-amp design [4, section 8.3] was used for comparison. The particular design parameters for the latter were supplied by [7]. The second op amp lacks rail-to-rail common mode range, but was judged to be a conservative reference design.

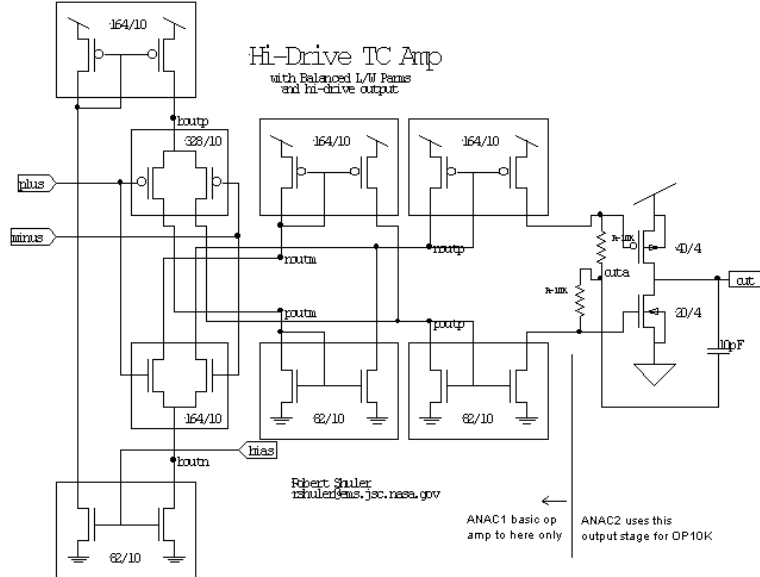


Figure 3 - OP10K Module for ANAC2

6 Signal Conditioning

Beginning at the front of the signal chain, we now consider each section. A standard 3-op-amp instrumentation amp circuit was used to convert differential inputs to single-ended. In this circuit, the gain is determined by a ratio of resistors. Simple transmission-gate switches were used to select resistors, and thus gains. Several sizes of these switches were drawn, and selected to contribute only a small percentage to the overall circuit impedance.

Since the circuit used has a minimum gain of 2x, on the second chip a voltage divider was provided which can be switched in to give a gain of 1x. This also allows handling of input signals greater than the 3.3 volt limits of the HP 0.5 μ process. Table 1 shows the gains possible with the second chip.

| GAINS/ RANGES: | no atten | atten |
|-------------------|--------------------|-------------------|
| low | 2 $\pm .75v$ | 1 $\pm 1.5v$ |
| high | 200 $\pm 7.5mv$ | 100 $\pm 15mv$ |

Table 1 - Gain Ranges for ANAC2

7 Low Pass Filter

The key element of this effort was incorporation of a low pass filter having the capability of a cutoff as low as 10 Hz, in reasonable area, with 100% on-chip components. Two poles of filtering per channel were included, with selectable cutoff frequencies of 10, 20, 50, 100, 250 and 500 Hz.

Surveys of available designs in 1994 revealed nothing in this area, and in 1996 a small project was funded by JSC at Texas A&M University, which resulted in a 2.0μ switched capacitor design, with pre- and post- anti-alias filters, having many of the desired characteristics [5]. However, this complex design did not fit well into our building block approach, and was not successfully assimilated.

Building on unpublished work from 20 years ago on programmable impedance amplifiers, the author developed a technique for actively manipulating the value of a capacitor. On subsequent search, this turns out to be known in the literature simply as a capacitor multiplier [6].

Several topologies present themselves for application of this circuit, and further refinement of the optimal point for extracting output to eliminate the need for buffer amplifiers was noted by [7]. Thus, one very low frequency pole per op amp stage is achieved using IC-compatible component sizes. The gain of the circuit shown in Figure 4 is always unity. The cutoff frequency can be varied by switching out capacitors of various sizes, or by changing the resistance ratio $R2/R3$. Both methods are used.

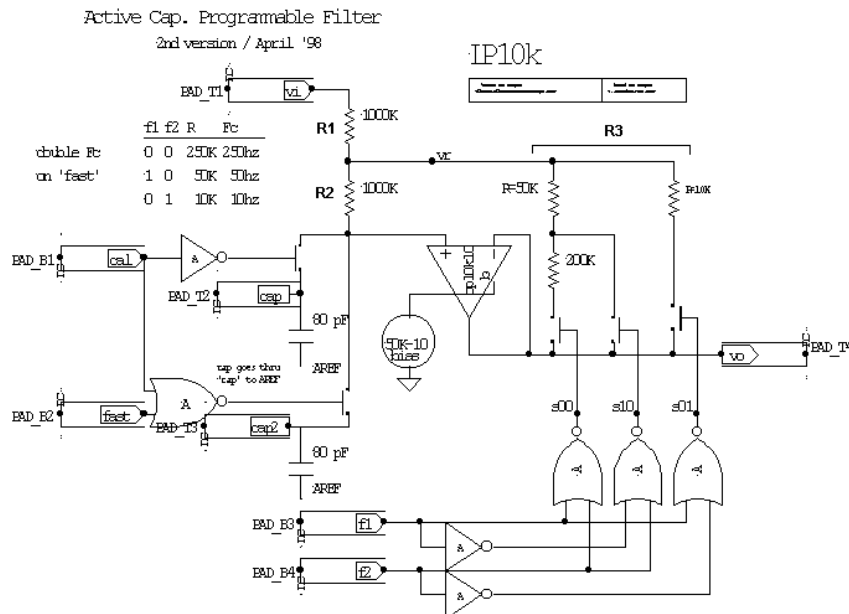


Figure 4 - Programmable Low Pass Filter Stage for ANAC2

8 Offset Reduction Strategy

A principal concern with the design of low-level instrumentation interfaces is the input-referenced offset or intrinsic error voltage of the initial gain stage. Additionally, a characteristic of the filter circuit just described is that the offset of the working op amp is multiplied by the same ratio R_2/R_3 that the capacitor is multiplied by. Thus offset of later stages in this design also become a performance limiting parameter.

As noted earlier, non-systematic (i.e., not consistent from one op amp to the next on-chip) offsets of 2 millivolts average were measured for ANAC1. Even more significant, the offset varied quite slowly, less than 0.2 millivolts per quarter hour. Even allowing for anticipated variation with temperature, the rate should still be relatively slow. This led to a design for ANAC2 in which both the differential inputs can be switched to AREF (1.6v) and the offset measured. This will be controlled by the host microcontroller software, and measurements can be taken as often as needed to obtain low error. The filter capacitor is switched out when offset is measured, so that the filter state is not disturbed, and the offset of the entire signal chain is measured at once. This value is then subtracted from subsequent measurement values to obtain the best zero-referenced signal conversions.

Even the above method still leaves much to be desired. If too many filter stages are used, or too high a capacitance multiplication, the offset can become large enough to place a full-scale signal out of supply limits. Further work toward a third generation test chip has been sponsored at Mississippi State University, along two directions. First, they are attempting to develop a ping-pong offset adjusted op amp stage which is simple enough to be adopted into our block methodology and re-utilized in more complex ASIC's. Second, they are planning to provide a general purpose op amp with higher drive capability than those used in ANAC2, so that lower overall resistance can be used in both instrumentation amp and filter stages. By selecting the appropriate amp type, either very high accuracy or very high circuit density can hopefully be attained, as the application requires.

9 Analog to Digital Conversion

Since 1000 s/s conversion rate is acceptable in this application, the simplest possible serial (i.e. ramp & counter based) A/D conversion was selected [4, section 10.5]. Due to low op amp gain, as mentioned previously, the ramp was not sufficiently accurate in ANAC1. ANAC2 uses both improved op amps and an improved ramp circuit, and attempts 10 bit conversions, which is the minimum requirement of most applications. Future circuits will require 12 bit converters, and the converter accuracy may have to be revisited yet again. The ramp generator is a simple integrator.

An interesting feature of the converter architecture is the absence of any analog multiplexing requirement. In ANAC2, each channel has its own comparator and counter. The ramp and timing signals are distributed to all channels on a chip. In ANAC1, there

was only one counter, but the comparator outputs were multiplexed via digital logic. This architecture is quite flexible. All the analog signals are kept local to a few analog blocks, minimizing noise and crosstalk.

10 AREF Generation

The analog reference signal ($AREF = 1.6\text{v}$) is generated on-chip using a simple stack of two P-N junctions. This worked well enough in ANAC1. For ANAC2, certain designs will sink more current into AREF, so the reference was buffered with an op amp. Provision is made for driving AREF also from off chip, either in case of problems, or if for some reason it is needed to have all chips using the same AREF.

11 Clock Generation

A simple RC based 20 MHz oscillator was used as a clock, and divided down to the 1.25 MHz operating frequency. Provision is made for using an external clock (if several chips are chained, only one clock can be used), and for shutting down the on-chip clock to make noise measurements. Digital section noise in the analog, mostly clock noise, proved to be about 0.1 to 0.2 volts in ANAC1. Due to other problems in ANAC1, it is not clear this actually would have caused measurement error. The clock noise is after all totally synchronous with the A/D conversion cycle. For ANAC2, the RC module decoupling was used as previously described. If this proves inadequate, power supply isolation will be used. Still further options are available, such as the SOI CMOS process now available through MOSIS, but the analog components will have to be re-designed to migrate to a completely different process.

12 Digital Output

The serial digital output is a 4-wire synchronous daisy chain bus. Each output drives only the input of the next chip, so there are no fanout considerations. The signals are CLOCK, GO, DATA and OK2SEND. The host microcontroller is assumed to be both the head and tail of the chain, sending the GO signal to initiate conversion, and sending OK2SEND to initiate read out. As each channel completes read out, it sends OK2SEND to the next channel, whether on the same chip or the next chip. For debug purposes, parallel digital outputs from one of the channels are provided. Obviously, in a building block approach, it is desirable to be able to replace the digital section with other types of interfaces, appropriate to each application.

13 Overall Architecture

Figure 5 shows the overall schematic architecture and layout of the 2-channel ANAC2 chip. By controlling the chip pin-out order, the automatic router was persuaded to place the two digital modules at the bottom of the layout, and the two input modules at the top, near the input pins. Another JSC organization is preparing an FPGA based circuit board

with LabView interface for thorough evaluation of ANAC2 over a range of sensor inputs and environmental conditions. Unpackaged parts would be used in an actual application.

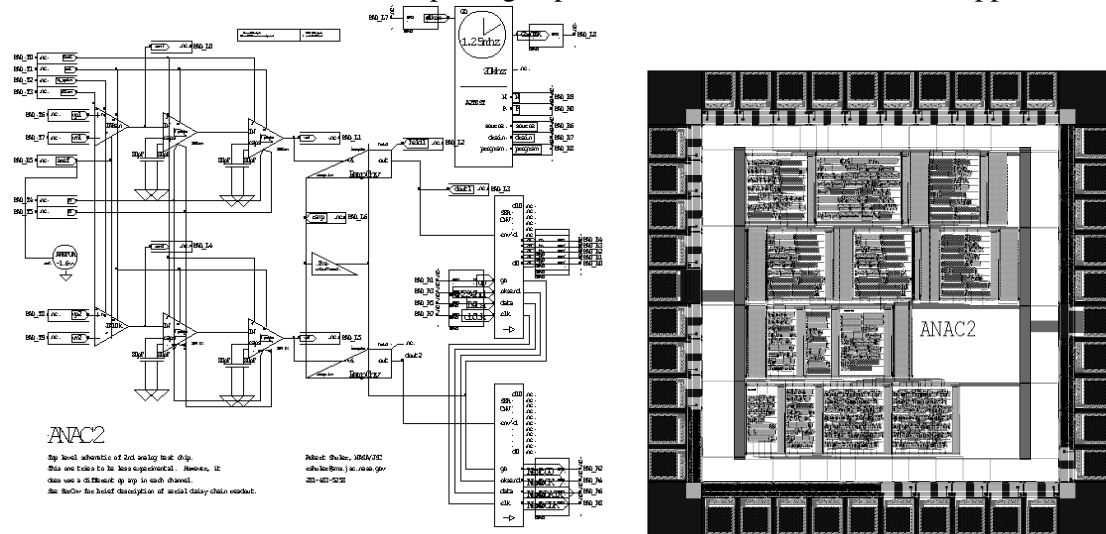


Figure 5 - Overall Schematic & Layout for ANAC2

14 Conclusion

The four most pressing problems with fully integrated CMOS digital sensor interface modules for use in space flight appear to be:

1. Radiation Tolerance
2. Low Pass On-chip Anti-Alias Filter
3. CMOS Op-amp Offset
4. Noise Coupling from Digital Circuits

The experimental results from the University of New Mexico demonstrate that radiation tolerance is solvable, and it is a matter of selecting and testing the degree of tolerance. When other functional requirements have been met, a future test chip in this series will be radiation tested, and the strategy amended in that area as necessary.

Experimental results from our own work (the ANAC1 chip) demonstrate an adequate solution to completely integrated low pass filters. Actually, ANAC1 demonstrated a cutoff as low as 2 Hz with very modestly sized passive components on-chip.

High performance low offset CMOS op amps continue to be a conundrum for researchers. ANAC1 results suggest adequate results can be achieved with simple adjustment strategies. Further investigation into improved schemes is on-going, and the question seems to be more keeping the complexity manageable than achieving the required targets.

Noise performance then appears the final unknown to be confronted. The ANAC2 chip should provide a more stable, accurate functionality base (through improved op amps and A/D) on which to measure noise, and tests a block decoupling strategy.

References

- [1] J. V. Osborn, et. al. "Total Ionizing Dose and Single Event Latchup Characteristics of Three Commercial CMOS Processes". Pre-publication copy of paper submitted to 1997 IEEE NASREC as late breaking news.
- [2] Jody W. Gambles. "A Path Toward Low Cost Rad-Tolerant Digital CMOS". 6th NASA Symposium on VLSI Design 1997.
- [3] Douglas Kearns. *Unpublished notes on analog design*. Tanner Research, Inc. 180 North Vinedo Ave., Pasadena, CA 91107.
- [4] Allen & Holberg. *CMOS Analog Circuit Design*. New York. Holt, Rinehart & Winston, 1987.
- [5] Jan-Michael Stevenson, Gunhee Han, and Edgar Sanchez-Sinencio. "A Low-Noise, Programmable Gain and Cutoff Frequency Data Acquisition Chip: Version Two". Texas A&M U., Dept. of EE, College Station, TX 77843-3128.
- [6] Horowitz and Hill. *The Art of Electronics*. 2nd Edition, 1989, p. 305.
- [7] Personal communication with Benjamin J. Blalock at Mississippi State University, NSF Engineering Research Center.