# Pulse Distortion in SET Measurements from Layout and Adjacent Signals

Robert L. Shuler[1], Bharat Bhuva [2], Balaji Narasimham[3]

[1]Avionic Systems Division, NASA Johnson Space Center, Houston, TX 77058
[2] Bharat Bhuva, Department of Electrical Engineering & Computer Science, Vanderbilt University, Nashville, TN
[3] Balaji Narasimham, Staff Reliability Scientist, Broadcom Corp., Irvine, CA

**ABSTRACT:**

We show that short pulses in bulk CMOS are dramatically and unexpectedly affected by surrounding signals and layout when propagating through the type of circuits used recently to capture and measure Single Event Transients.

## I. BACKGROUND

Single Event Transients (SETs) are a major source of errors in CMOS circuits exposed to radiation environments. These result in Single Event Upset (SEU) errors when they occur within a storage element and are of sufficient duration to change the state of the memory cell. SETs also occur in combinational logic, and result in an SEU if they occur with a timing and duration to be captured on a clock edge. Both types of errors depend on the duration and propagation properties of SETs. Some Radiation Hardened by Design (RHBD) circuit techniques for mitigating SEUs also depend on the duration and distribution of SETs. Therefore, investigators have attempted to measure SETs by various methods.

Eaton, et. al. [1] used a tunable latch technique, which had to be re-tuned for each different length of pulse to be measured. Narasimham, et. al. [2] shortly thereafter proposed a method to freeze a pulse propagating through a chain of inverters, also known as capture latches. This had the advantage of being able to measure a variety of pulse lengths at once, but had to be stimulated with a controllable source such as a laser. The method had a measurement resolution of 900 picoseconds (ps) using 1.5 micron technology, and could measure a minimum pulse of 900 ps. Earlier, Paschalidis, et. al. [3] reported using a string of current starved inverters to measure very short pulses, including pulses from radiation event sensors. His method used a controllable absorption rate, and measured the number of inverter stages required to absorb a pulse, achieving a 300 ps resolution using a 0.8 micron process, after all calibration issues are taken into account. Paschalidis did not specify the shortest pulses that could be measured.

Shuler, et. al. [4] used an "ion collector" consisting of 16 parallel chains of 15 inverters merged through NAND gates, to collect and propagate SETs into Narasimham style capture latches, to collect and measure SETs from heavy ions in a particle beam. Using 0.35 micron technology, the capture latches yielded a 300 ps resolution, and were able to measure pulses as short as 300 ps. Narasimham, et. al. [5] then measured SETs in 130 nm and 90 nm, using single chains of inverters for ion collectors, or "target circuits." These were of length 110 inverters for 130 nm, and 1000 inverters for 90 nm. Analysis of these results depended on simulations that showed pulses (SETs) of greater than 180 ps and 150 ps respectively for 130 nm and 90 nm propagated without attenuation. Capture latch resolution (stage delay) was measured at 120 ps and 100 ps respectively using ring oscillators. No direct measurement of pulse propagation through the target (ion collector), or calibration other than the ring oscillator was reported, and only one type of circuit layout style was used.

In the same time period, papers appeared challenging the consistency of pulse propagation through inverter chains, based on experimental data, with Ferlet-Cavrois [6] reporting the broadening of 200 ps pulses into the nanosecond range in chains of 800 inverters in 130 nm SOI. This was followed by Wirth, et. al. [7] reporting in more detail on circuits similar to those used by Ferlet-Cavrois, including both SOI and bulk experiments. Wirth essentially shows that the kind of broadening he is observing results from load asymmetries, and for pulses in the range of 700 ps it is not observed in a uniform inverter string. In chains with extra loading on alternate stages, pulses of one polarity are broadened and pulses of the other polarity are absorbed, much like in Paschalidis' original measuring chains, which used deliberate narrowing to measure the pulses. Massengill [8] confirms the effect of even-odd load sequencing with a theoretical analysis, showing this type of broadening (or narrowing) to be due to CMOS device hysteretic effects.

Meanwhile, the present set of collaborators were applying the ideas of inverter chain ion collectors and capture latches to attempt to compare the SET characteristics of various layout styles, with and without guard rings, guard drains, and other features, and were also attempting to directly measure charge sharing, as described from modeling and laser results by Amusan [9]. This effort used strings of 240 inverters in 180 nm technology, several different layout styles which were compared, and interleaved circuits for the charge sharing measurement. Several types of calibration circuits were included to make sure we could compare these different circuits fairly over a range of pulse widths. It is the unexpected results of those calibrations on which we here report. These results suggest that there are effects on short pulses less than 1 ns, not heretofore reported that greatly affect the length of pulses propagated and measured using inverter chains and capture latches, and affect the utility of such measurements. These effects show up prominently when comparing the different layout and circuit topologies, but are hard to see when looking at a single circuit type. We report also some simulation analysis of conjectured reasons for the effects, and propose circuit techniques to minimize them.

## II. EXPERIMENT DESIGN

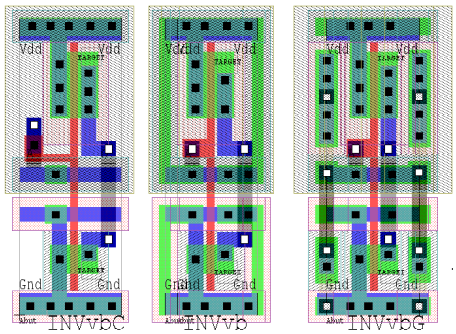


Figure 1: Layout – unprotected (left) guard ring "A" cells (center), guard drain"G" cells (right)

Figure 1 shows the types of layout compared. The guard ring layout has substrate contact diffusion surrounding both P and N regions of the inverter. It is fully contacted above and below, but not on the sides. This we call "A" type layout. The guard drain "G" layout, suggested by Gambles [10], has substrate contacts (guard bars) above and below the P and N regions, but has supply side contacts (guard drains) on the sides separating adjacent cells. In some cases guard drains will sweep out charge more efficiently, but at deep submicron using them in wells may not be advantageous due to well collapse (Narasimham [11]).

Normal or “single string” target circuits consisted of chains of 240 inverters of one or the other of the above types, in an isolated block. All capture latch circuits were identical, and used guard ring “A” style layout, each in its own block. A second set of experiments, designed to measure charge sharing, used three strings of 240 inverters in each target, connected to three sets of capture latches. These inverter strings were interleaved in the style shown in Figure 2, so that each inverter is adjacent to inverters in different strings. The idea is that if a particle strike induces an SET in two or more inverters, the resulting pulses will be in logically different strings and will be captured and measured independently.

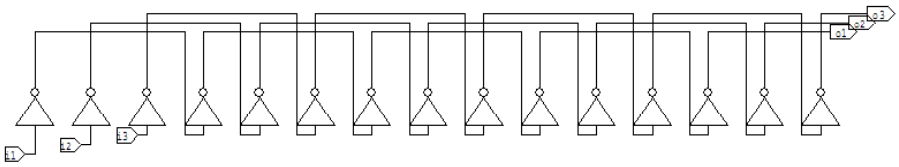

Figure 2: Interleaved inverter strings

Figure 3 shows calibration of capture latches. While it differs from the desired straight line, it is consistent and can be easily used to determine true width of measured pulses from capture latch counts. More detail on capture circuit design and calibration will be included in the full paper.

**III. EXPERIMENTAL RESULTS**

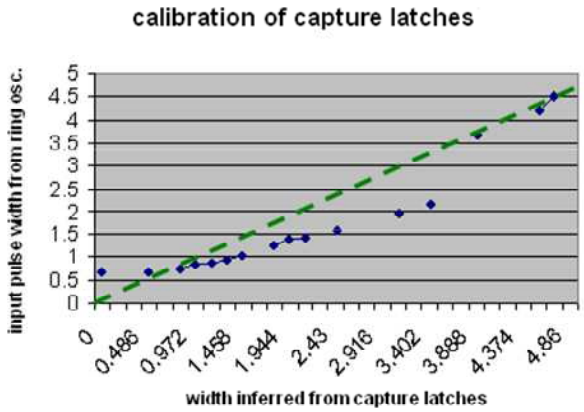


Figure 3: Calibration of Capture Latches

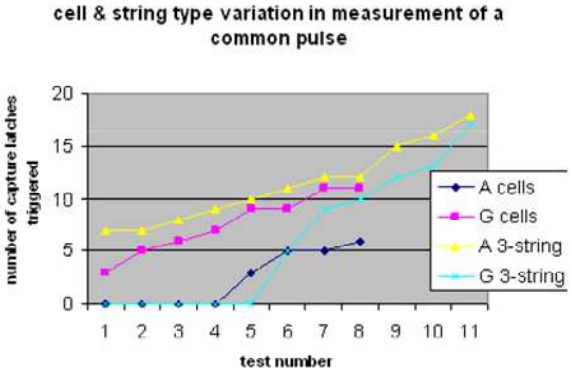


Figure 4: Variation in pulse absorption

Figure 4 shows the measured pulse width, in capture latch counts, for a common input test pulse routed to the first inverter of all target circuits. Additional data on unprotected inverters will be shown in the full paper. For the single string circuits, it is apparent the A cells are absorbing short pulses below 5 capture latch counts, or about 750 ps. Then there is a strange, nearly constant, difference between A and G cells for longer pulses. For the interleave 3-string targets, the pulse was sent down all three strings. In this case, it is the G cells that appear to absorb short pulses, but for longer pulses the A and G 3-string case converges. We can see immediately the layout may make some difference. The substrate contacts may slightly increase capacitance to ground. But what explains the interleaved case? The inverters are all surrounded by identical inverters. But they are carrying simultaneous signals in the 3-string case, and not in the single string case. The spice simulation shown in Figure 5 suggests that a small capacitive coupling between adjacent inverters may set up an interaction between adjacent signals that allows them

to influence one another. The center string inverter is supported on both sides and sees less load, while the outer inverters are opposed on one side. Sidewall layout would affect this coupling.

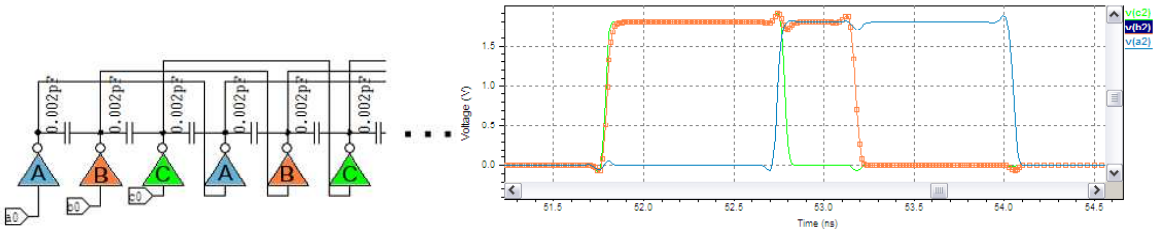


Figure 5: Spice simulation results for 3x240 interleaved inverters with .002pF coupling

## IV. CONCLUSION

Data from this chip could hardly be relied upon. Without knowing exactly where the SET was injected, and having an accurate model, the effect cannot be removed by calibration. The effects were noticed in these experiments because the comparisons were available. However, we believe these effects may be significant in other reported results, but not noticed due to the lack of a reference comparison. For future investigations, we suggest returning to the merger of shorter strings, and further work to clarify at what lengths the effect can be ignored. We have experiments in process to try a more sophisticated alternation of inverters for charge sharing measurement, shown in Figure 6, to resolve adjacent node interaction, but there will still be a practical limit on string length due to the single string effects.

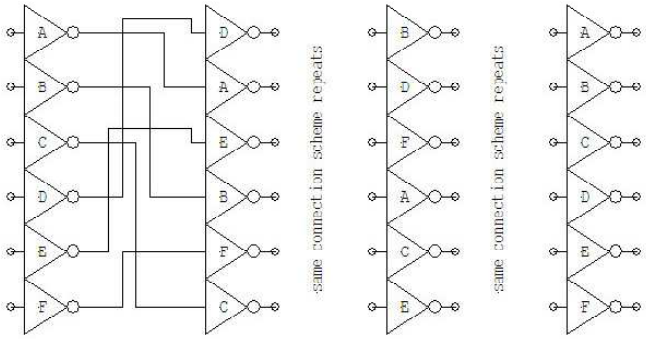


Figure 6: Interleaved and alternated inverter strings

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